FP7721BX2

Integrated Switch Dual Channel Charge Pump

Description

The FP7721BX2 is an integrated power supply solution optimized for small to medium size thin-film transistor (TFT) liquid crystal displays (LCD's). Primarily intended for smart phone and tablet LCD panel's driver IC.

The positive charge pump has an internal switch and typically can support output current up to 100mA at V_{CI}=3.3V.

Negative charge pump has an internal switch to generate -1 ratio of VSN and typically can support output current up to 100mA at V_{CI}=3.3V.

The pump clock can be synchronized with external signal from driver IC or can be generated by internal circuit fixed to 600kHz.

The FP7721BX2 is available in a thin 12-pin 2.4x1.5 mm UTDFN green package.

Features

- 2.5V to 4.8V Input Supply
- Generate two output voltage, positive voltage (VSP) and -1 ratio of negative voltage(VSN)
- Only 5 external capacitors
- UTDFN-12 (2.4mmx1.5mm) Exposed Pad Package

Applications

- TFT LCD for smart phone and tablet LCD panel's driver IC

Pin Assignments

Package (UTDFN-12)(2.4mm x 1.5mm)

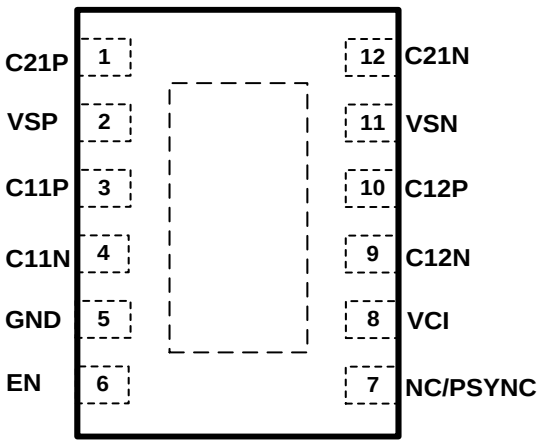


Figure 1. Pin Assignment of FP7721BX2

Ordering Information

FP7721□

Package Type
BX2: UTDFN-12 (2.4mmx1.5mm)

Marking Code

Part Number	Product Code
FP7721BX2	FP5

Typical Application Circuit

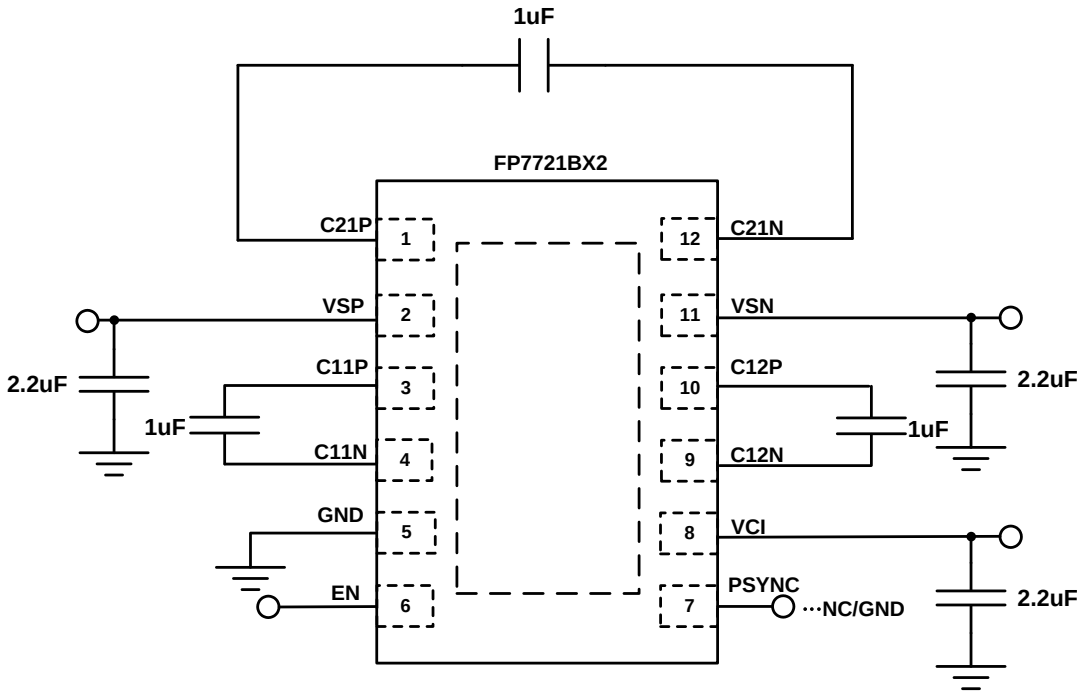


Figure 2. Pump clock fixed to 600 kHz (generated by internal circuit) for FP7721BX2

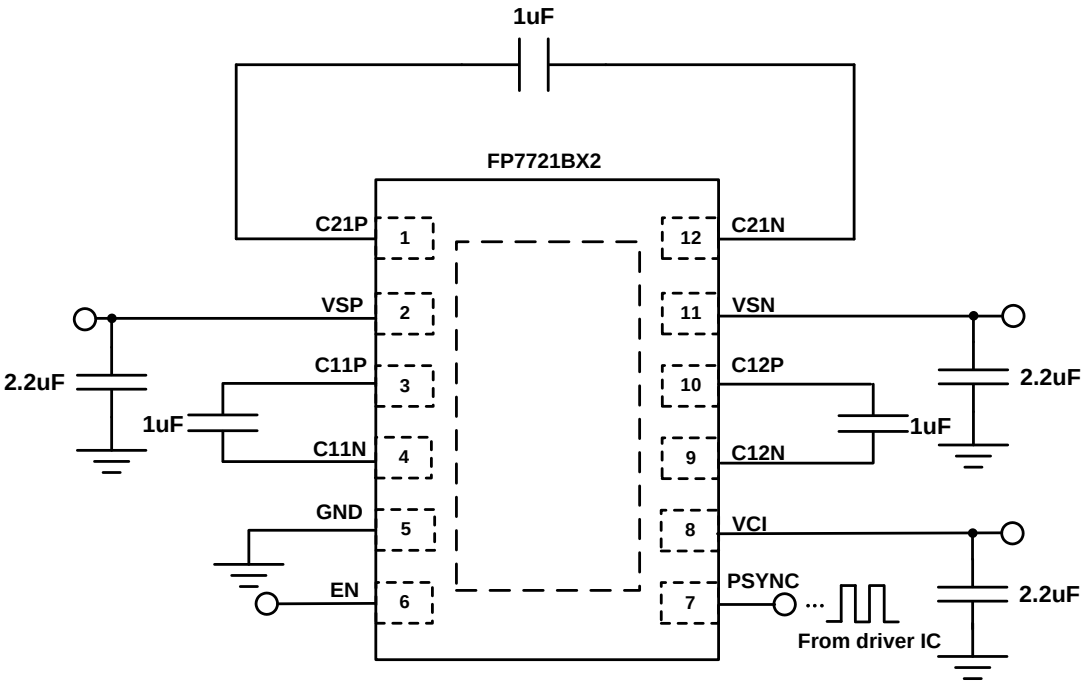


Figure 3. Pump clock synchronized with driver IC(Duty=50%) for FP7721BX2

Functional Pin Description

Pin No.	Pin Name	I/O	Pin Function
1	C21P	I	Capacitor connection pin for the VSN.
2	VSP	O	Positive voltage output pin (VSP).
3	C11P	I	Capacitor connection pin for the VSP.
4	C11N	I	Capacitor connection pin for the VSP.
5	GND	P	Ground pin.
6	EN	I	Enable pin.
7	PSYNC	I	PSYNC pin connect with GND or use external clock from driver IC for FP7721BX2
8	VCI	P	Power supply input pin.
9	C12N	I	Capacitor connection pin for the VSP.
10	C12P	I	Capacitor connection pin for the VSP.
11	VSN	O	Negative voltage output pin (VSN).
12	C21N	I	Capacitor connection pin for the VSN.

Block Diagram

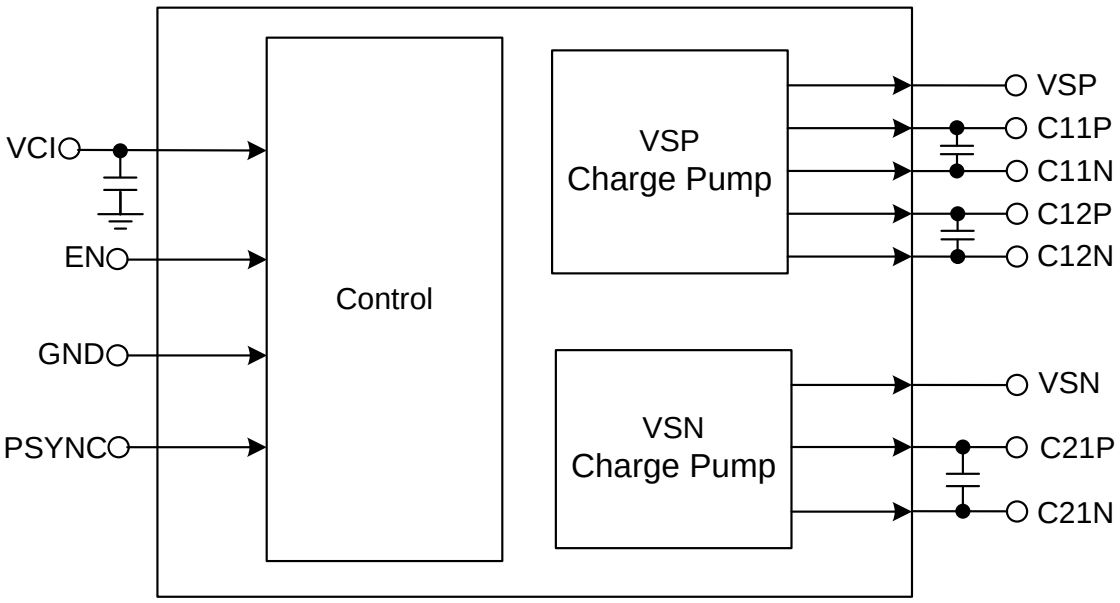


Figure 4. Block Diagram of FP7721BX2

Absolute Maximum Ratings

- VCI ---------- -0.3V to 6V
- Control signal voltage ---------- -0.3V to 6V
- VSP ---------- 0V to 6V
- VSN ---------- 0V to -6V
- Operating Junction Temperature Range (T_J) ---------- -40°C to +125°C
- Operating Temperature Range (T_{OP}) ---------- -40°C to +85°C
- Storage Temperature Range ---------- -55°C to +150°C
- Lead soldering Temperature Range (10 seconds) ---------- -40°C to +125°C

Note1：Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

Electrical Characteristics

(V_{IN}=3V, TA=-40°C to 85°C, unless otherwise specified. Typical values are tested at 25°C ambient temperature)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply						
Input Voltage	V_{CI}		2.5		4.8	V
VCI Under Voltage Lockout (UVLO)	V_{UVLO}	VCI Rising	2	2.2	2.4	V
		Hysteresis		200		mV
Standby Current	$I_{STANDBY}$				2	uA
Output Voltage VSP						
Output Voltage Range	V_{SP}	VCI=3V. Io=0mA	5.6		6	V
Output Current Capability		VCI=2.8V		35		mA
		VCI=3V		60		mA
		VCI=3.3V		100		mA
Output Voltage VSN						
Output Voltage Range	V_{SN}	VCI=3V. Io=0mA	-5.6		-6	V
Output Current Capability		VCI=2.8V		35		mA
		VCI=3V		60		mA
		VCI=3.3V		100		mA
LOGIC EN/PSYNC						
Threshold Voltage	VIH		1.5			V
	VIL				0.5	V
PSYNC Frequency			50			kHz
Internal Pump Clock Frequency				600		kHz
Enable Pull down Resistor				300		kΩ

Power On/Off Sequence

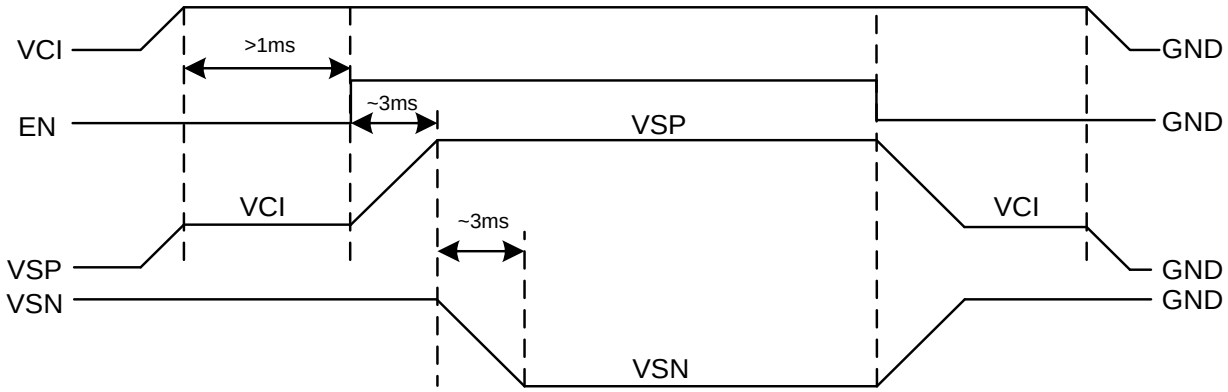


Figure 5. Power sequence of pump clock used internal circuit for FP7721BX2

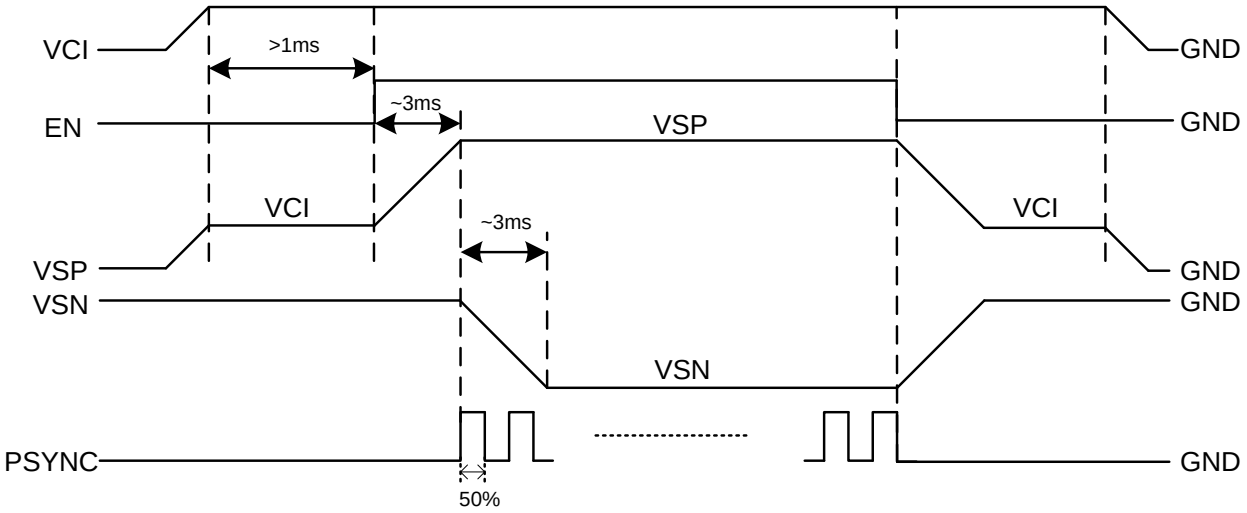


Figure 6. Power sequence of pump clock used synchronized signal from driver IC for FP7721BX2

Typical Performance Curves

V_{IN}=3V/3.3V, T_A=+25°C, internal clock, unless otherwise noted.

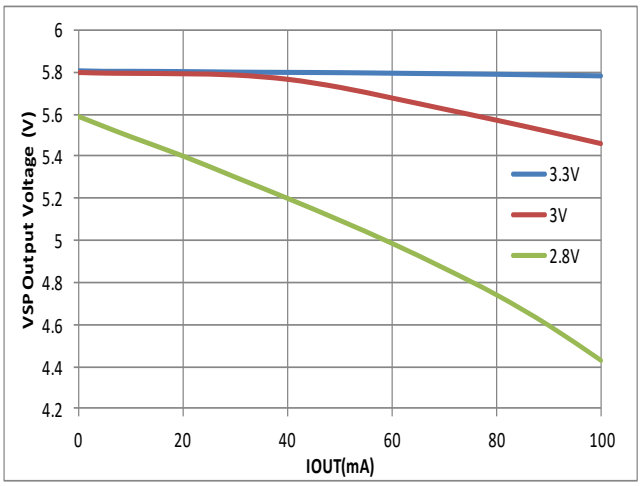


Figure 7. VSP's Output Voltage vs. Output Current

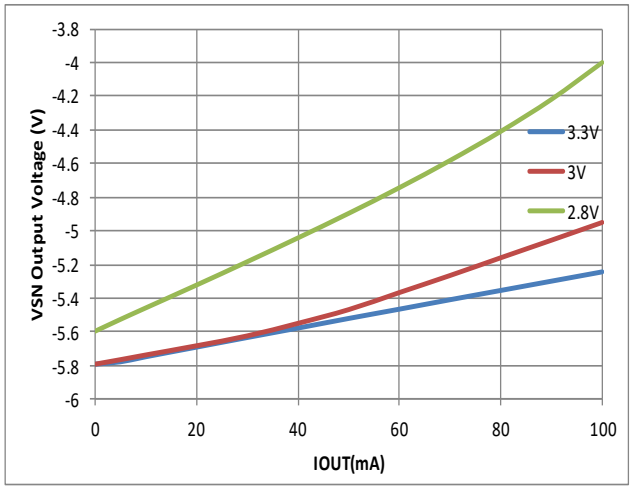


Figure 8. VSN's Output Voltage vs. Output Current

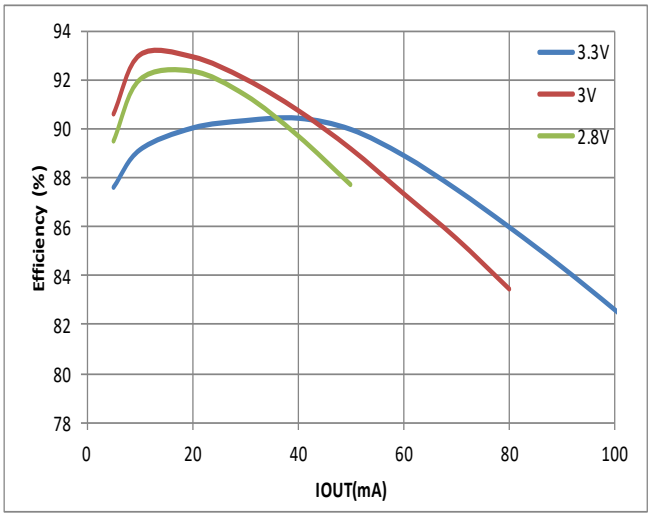


Figure 9. Efficiency vs. Output Current

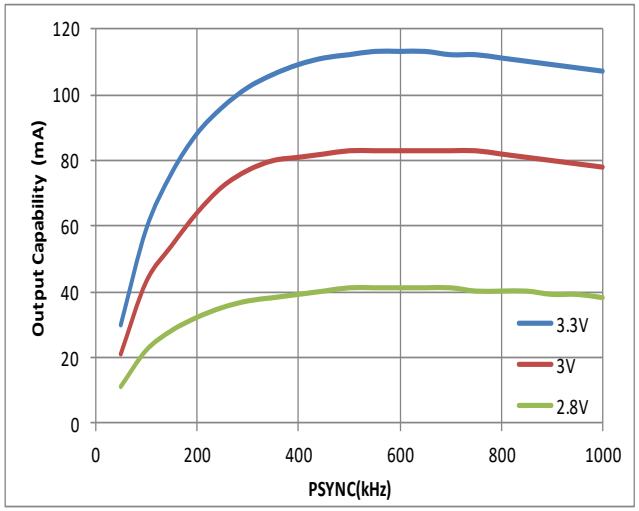
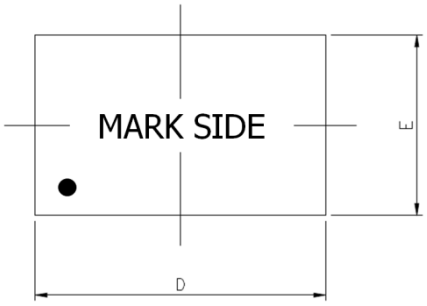
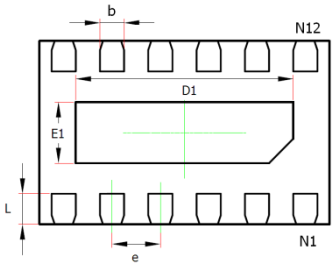


Figure 10. PSYNC Frequency vs. Output Capability

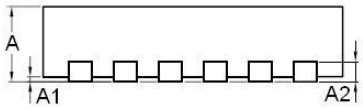
Outline Information

UTDFN- 12L 2.4mm x 1.5mm (pitch 0.4 mm) Package (Unit: mm)

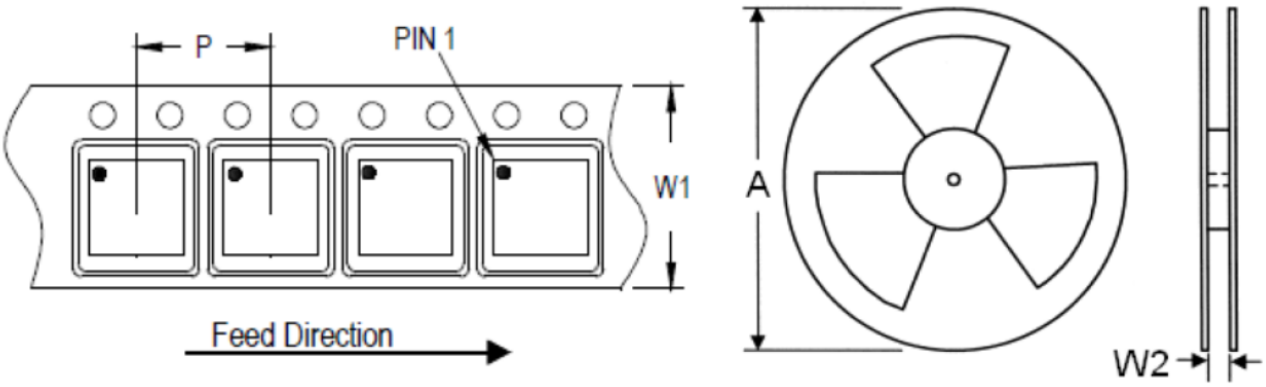




SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.40	0.55
A1	0.00	0.05
A2	0.10	0.20
D	2.30	2.50
E	1.40	1.60
L	0.20	0.30
b	0.15	0.25
e	0.35	0.45
D1	1.70	1.90
E1	0.40	0.60



Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
8	4	7	180	8.4	300~1000	3,000

Life Support Policy
Jadard's products are not authorized for use as critical components in life support devices or other medical systems..

Layout Considerations

PCB layout is very important to design charge pump circuits. The following layout guide lines should be strictly followed for best performance of the FP7721BX2.

- **Pin1 & P12** is Negative Charge pump, **C4** Provide energy for VSN, Place the **C4** components to **Pin1 & P12** as close as possible.
- **Pin3 & Pin4** is Positive Charge pump, **C6** Provide energy for VSP, Place the **C6** components to **Pin3 & P4** as close as possible.
- **Pin9 & Pin10** is Positive Charge pump, **C2** Provide energy for VSP, Place the **C2** components to **Pin1 & P12** as close as possible.
- **Pin 8** requires a stable and clean Input voltage.Place the capacitor **C1** stable input voltage. Place the **C1** components to pin8 as close as possible.

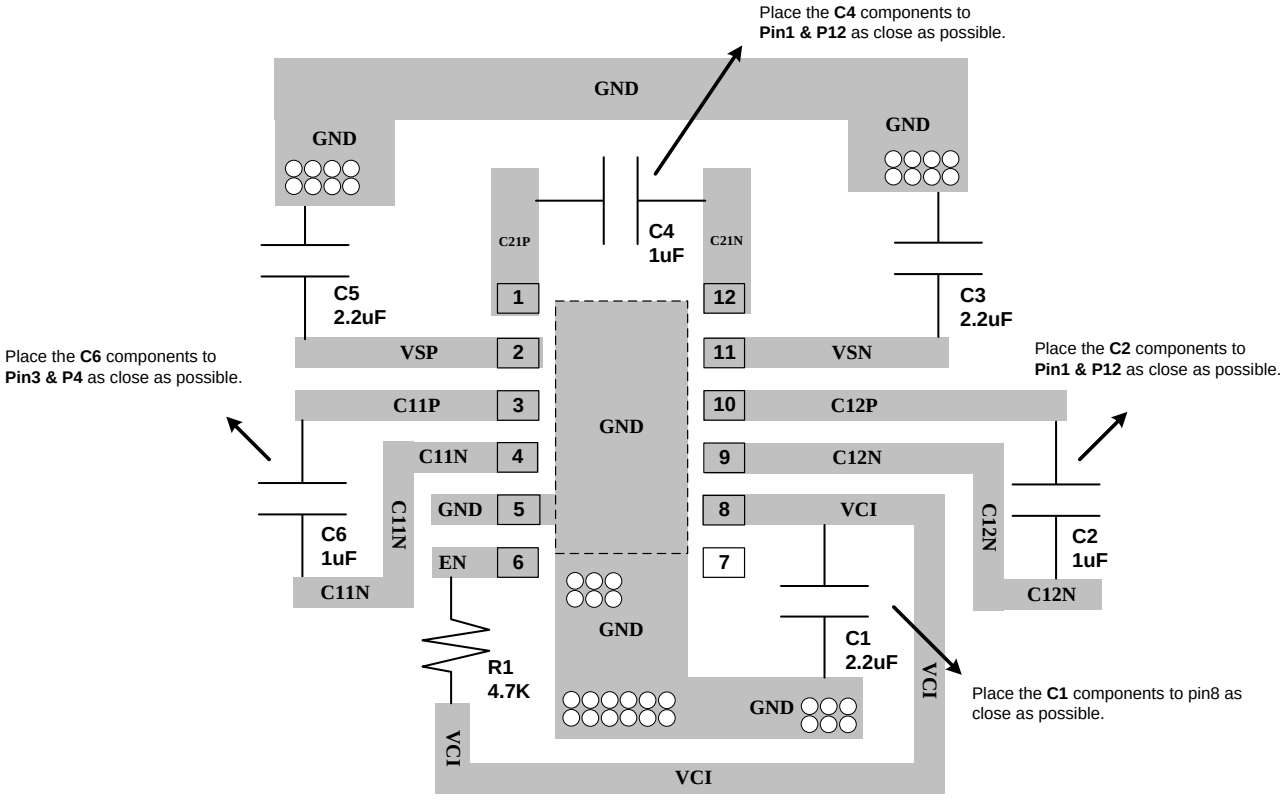


Figure 11. Layout trace guideline